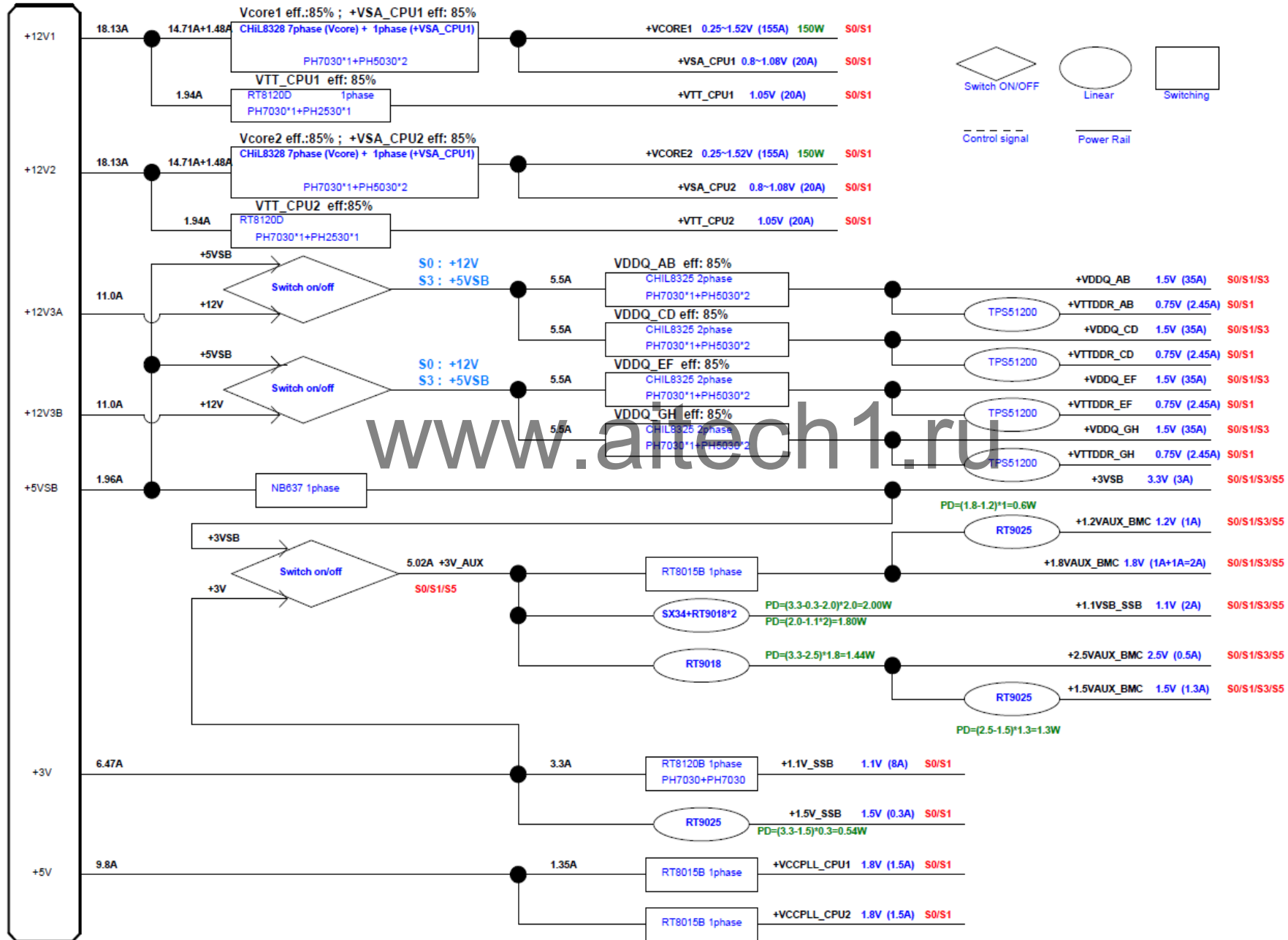
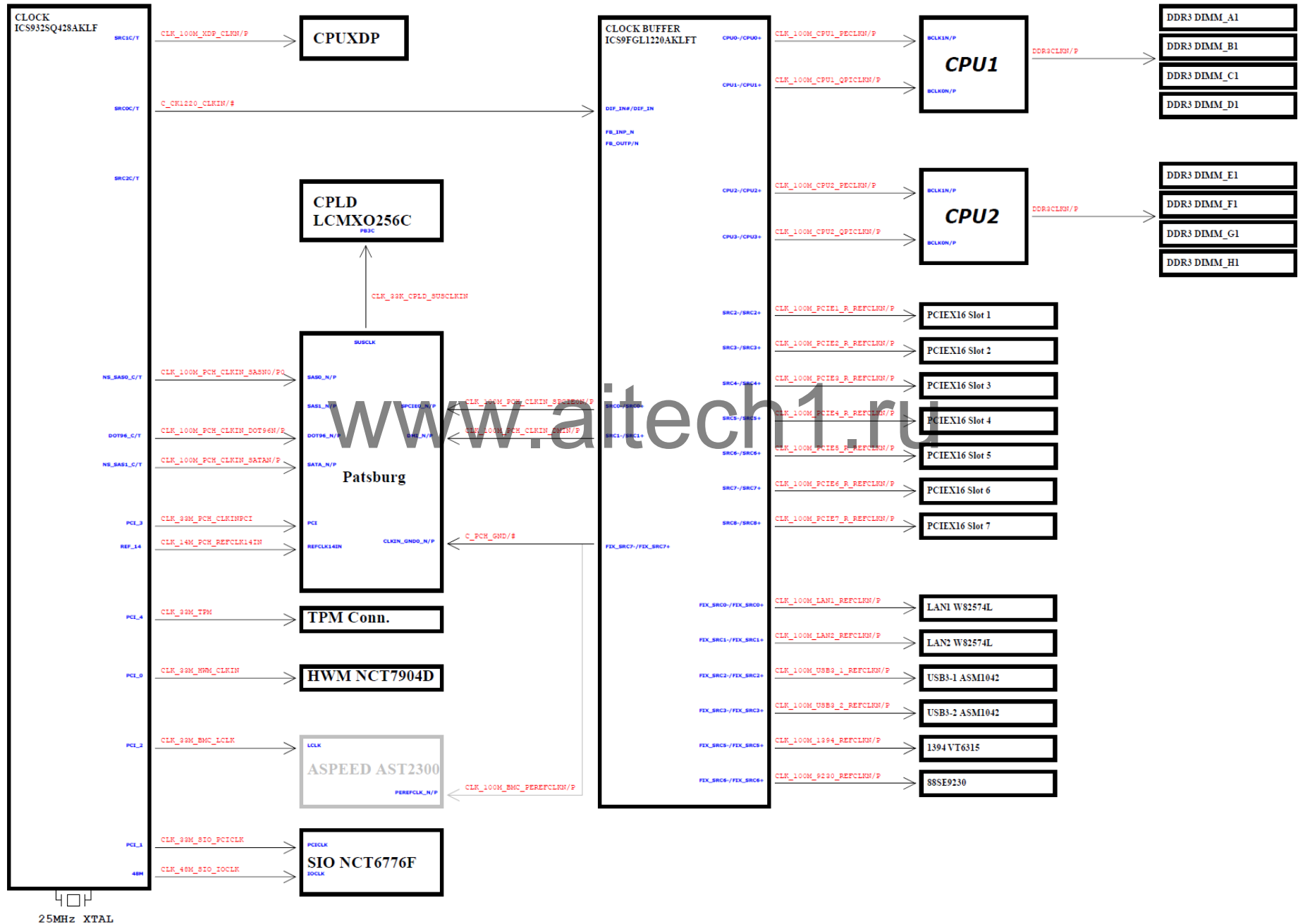


POWER FLOW

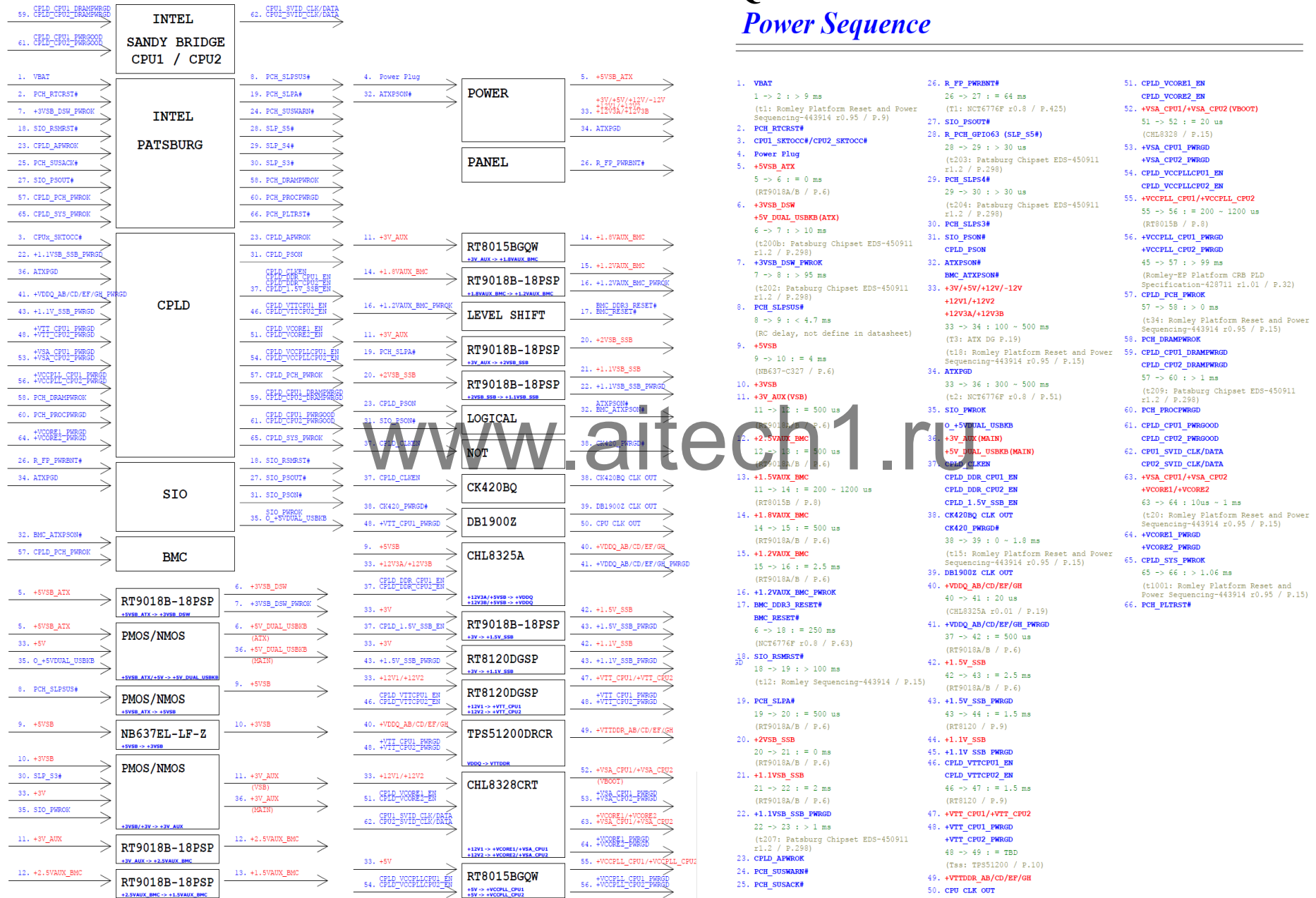


Clock Distribution



POWER ON SEQUENCE

Power Sequence



Power Map

POWER	S0	S1	S3	S4	S5	ENABLE	S0	S1	S3	S4	S5	SOURCE
+VCORE1	ON	ON	OFF	OFF	OFF	CPLD_VCORE1_EN	H	H	L	L	L	+12V1
+VSA_CPU1	ON	ON	OFF	OFF	OFF	CPLD_VCORE1_EN	H	H	L	L	L	+12V1
+VCORE2	ON	ON	OFF	OFF	OFF	CPLD_VCORE2_EN	H	H	L	L	L	+12V2
+VSA_CPU2	ON	ON	OFF	OFF	OFF	CPLD_VCORE2_EN	H	H	L	L	L	+12V2
+VDDQ_AB	ON	ON	ON	OFF	OFF	CPLD_DDR_CPU1_EN	H	H	H	L	L	+12V3A +5VSB
+VDDQ_CD	ON	ON	ON	OFF	OFF	CPLD_DDR_CPU1_EN	H	H	H	L	L	+12V3A +5VSB
+VDDQ_EF	ON	ON	ON	OFF	OFF	CPLD_DDR_CPU2_EN	H	H	H	L	L	+12V3B +5VSB
+VDDQ_GH	ON	ON	ON	OFF	OFF	CPLD_DDR_CPU2_EN	H	H	H	L	L	+12V3B +5VSB
+VTTDDR_AB	ON	ON	OFF	OFF	OFF	+VTT_CPU1_PWRGD	H	H	L	L	L	+VDDQ_AB
+VTTDDR_CD	ON	ON	OFF	OFF	OFF	+VTT_CPU1_PWRGD	H	H	L	L	L	+VDDQ_CD
+VTTDDR_EF	ON	ON	OFF	OFF	OFF	+VTT_CPU2_PWRGD	H	H	L	L	L	+VDDQ_EF
+VTTDDR_GH	ON	ON	OFF	OFF	OFF	+VTT_CPU2_PWRGD	H	H	L	L	L	+VDDQ_GH
+VCCPLL_CPU1	ON	ON	OFF	OFF	OFF	CPLD_VCCPLLCPU1_EN	H	H	L	L	L	+5V
+VCCPLL_CPU2	ON	ON	OFF	OFF	OFF	CPLD_VCCPLLCPU2_EN	H	H	L	L	L	+5V
+VTT_CPU1	ON	ON	OFF	OFF	OFF	CPLD_VTTCPU1_EN	H	H	L	L	L	+12V1
+VTT_CPU2	ON	ON	OFF	OFF	OFF	CPLD_VTTCPU2_EN	H	H	L	L	L	+12V2
+1.1V_SSB	ON	ON	OFF	OFF	OFF	+1.5V_SSB_PWRGD	H	H	L	L	L	+3V
+1.5V_SSB	ON	ON	OFF	OFF	OFF	CPLD_1.5V_SSB_EN	H	H	L	L	L	+3V
+1.1VSB_SSB	ON	ON	ON	ON	ON	PCH_SLPA#	H	H	H	H	H	+3V_AUX
+1.8VUX_BMC	ON	ON	ON	ON	ON	+3V_AUX	H	H	H	H	H	+3V_AUX
+1.2VUX_BMC	ON	ON	ON	ON	ON	+1.8VUX_BMC	H	H	H	H	H	+1.8VUX_BMC
+2.5VUX_BMC	ON	ON	ON	ON	ON	+3V_AUX	H	H	H	H	H	+3V_AUX
+1.5VUX_BMC	ON	ON	ON	ON	ON	+2.5VUX_BMC	H	H	H	H	H	+2.5VUX_BMC
+3VSB	ON	ON	ON	ON	ON	+5VSB	H	H	H	H	H	+5VSB
+3V_AUX	ON	ON	ON	ON	ON	PCH_SLPS3# SIO_PWROK	H	H	H	H	H	+3VSB +3V
+5VSB	ON	ON	ON	ON	ON	PCH_SLPSUS#	H	H	H	H	H	+5VSB_ATX
+3VSB_DSW	ON	ON	ON	ON	ON	+5VSB_ATX	H	H	H	H	H	+5VSB_ATX
+5V_DUAL_USBKBMS	ON	ON	ON	ON	ON	O_+5VDUAL_USBKBB	H	H	H	H	H	+5V +5VSB_ATX

Voltage & Signal Measure Point

